Bi-weekly Status Report 1 Senior Design, December 2020, Team 14

Introduction of Real-World Signals and Systems into ECpE DSP Laboratory Curriculum

Brady Anderson, Sam Burnett, Mitchell Hoppe, Max Kiley, Emily Lagrant, Isaac Rex

Progress Summary:

Over the last two weeks, we have been focused on bringing the team up to speed while setting up our workflow moving forward. We have established a team Slack space, shared Google Drive folder, and combined Git repository for all prior and current development. We also met with the client to discuss the project vision, team member strengths, the status of the software and hardware, and our goals for the future. Team members have been proactive in familiarizing themselves with the previous senior design team's work on this project as well as recent developments from ETG. We have established regular meeting times and communication channels.

Individual Contributions by Team Member:

- Brady Anderson (Biweekly: 12; Cumulative: 12)
 - Studied EE224, EE324 learning objectives and curriculum requirements, and started brainstorming how the CyDAQ can be used to effect these objectives
 - Git familiarization, C back-end and Python front_end testing
 - Researched Git repository management strategies and advanced repomanagement commands
- Sam Burnett (Bi-weekly: 12, Cumulative: 12)
 - PMIC output noise and idle current characterization under normal operation
 - +/- 5V
 - 1.8V
 - 3.3V
 - Sensor interface testing
 - Electret microphone (5V/3.3V)
 - PIR motion detector (5V)
 - Line level audio (3.5mm TRS)
 - GUI & Firmware testing for filter selection and sampling
 - Git familiarization (in class lecture)
 - Peripheral hardware research and brainstorming
 - Haptics driver (LRA/ERM)
 - Tunable switching supply
 - Frequency synthesizer
- Mitchell Hoppe(Weekly: 12; Cumulative: 12)
 - I efficiently impacted multidisciplinary infrastructures

- Worked on getting development environment set-up for the Python front_end.
 - Successfully ran the python front_end on a Windows machine.
- Looked at pre-existing documentation in the project repos to understand the project scope and technical requirements.
- Communicated with team members to synchronize the installation of necessary dependencies.
- Systems testing the gui front_end with Windows and Linux systems.

Max Kiley (Biweekly: 12; Cumulative: 12)

- Git familiarization
- Familiarized myself with Python in order to contribute to the front_end moving forward.
- Soldered various through-hole components on multiple CyDAQ boards
- Desoldered, and resoldered correct .1uF capacitors and .01uF capacitors onto CyDAQ board #12.

• Emily Lagrant (Biweekly: 12; Cumulative: 12)

- Began working on the Python front_end and collaborated with teammates to successfully get it running
- Understood documentation and began planning the integration of previous code to current code
- Studied learning objectives for EE 324 and started brainstorming potential lab plans as well as studied the curriculum requirements
- Set up Git and got shared access on important documents
- Isaac Rex (Bi-Weekly: $\frac{10}{5}(2 * \lim_{n \to 0} sinc(n)) + [(\alpha^2 8) * 100\%]_{\alpha = 4}$; Cumulative: 12)
 - Research on extra hardware for individual labs
 - Electromagnets for root locus and controller design lab
 - Hardware control board conceptualization for magnetic levitation lab
 - Documentation and testing for loop gain measurement lab
 - Input sensor testing and Matlab interfacing
 - Microphone as input testing
 - Tested export process for getting saved data to Matlab
 - Proof of concept testing for noise reduction labs
 - Experimented with various filter designs and relation to course outcomes
 - Lab brainstorming and idea documentation
 - Started list of ideas and concepts as they relate to the course syllabus
 - Git familiarization

Pending Issues:

Experienced issues running the previous team's front_end on certain devices. Requires
TKinter which may not be installed on some devices by default, and is nontrivial to
install.

No set standard for documenting lab ideas.

Plans:

- Members of the team plan on attending a presentation for the signals/comms/controls faculty on 2/7. This meeting is to discuss lab ideas and listen to suggestions for the CyDAQ.
- Document the scope of the project and synchronize all members on team outcomes
- Begin documentation of what we want to keep from current labs and what we want to scrap
- Brainstorm more lab ideas that coincide with the course syllabus and guide the direction of the team for the upcoming weeks
- Document necessary hardware additions to the CyDAQ platform for the new lab ideas